FDSOI platform for quantum computing

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Abstract—Si-based qubits are considered the most promising experimental system for scaling quantum computing. For the first time, FDSOI CMOS technology is demonstrated as the platform to co-integrate hole and electron spin qubits with cryo-electronics. For cryo-control, we show voltage gain as high as 75dB for long devices, noise of $10^{-11}V^2{\cdot}\mu m^2/Hz$ and 1.29mV·µm threshold voltage variability. We propose a standard cell for two-qubit gates on commercial 22FDX® and show double quantum dot features. Finally, we demonstrate hole and electron qubits on the same FDSOI technology with a manipulation speed of 1µs and coherence time of 40µs (Hahn echo), respectively.

I. Introduction

Rapid advancements in quantum computing (QC) have boosted the exploration of semiconductor technologies to enhance qubit scalability [1]. Fully Depleted Silicon-On-Insulator (FDSOI) has emerged as a promising technology due to its strong electrostatic control over the channel, reduced variability, analog performance, and lower power consumption [2, 3]. The co-integration of qubits and control electronics is essential for scalable, high-performance, QC systems. Hole and electron spin qubits [4, 5] as well as cryogenic circuits for control and readout [6, 7] have both been demonstrated on FDSOI. For the first time we discuss the use of FDSOI as a base for a quantum-system-on-chip (QSoC), where transistors and qubits are integrated on the same chip, as shown in Fig.1.

In this paper, we highlight the co-integration challenges for QSoC, such as limited cooling power, sensitivity to disorder and physical effects, all of which must be considered in future cryogenic FDSOI modeling and design kits. With this in mind, we review the many opportunities to leverage FDSOI's advantages in QC architectures. We then round out the discussion with experimental results that demonstrate the feasibility of FDSOI-based qubits, highlighting key metrics such as charge readout fidelity, tunnel coupling (t_c) control, charge noise and reliability.

II. Devices and Setup

Devices in Section III were fabricated in commercial FDSOI foundries, using a standard CMOS processes flow. Devices in Section IV were fabricated at CEA-Leti and correspond to state-of-the-art (SoA) FDSOI qubit devices, where the process flow deviates very little from standard CMOS technology. Measurements were performed using probestations, home-built cryogenic dipsticks and dilution refrigerators. All devices were processed on 300mm wafers.

III. Cryo-CMOS and Co-Integration

In this section, we present analog parameters for FDSOI MOSFETs down to 4.2K and discuss the challenges of intersubband scattering (ISS) and the self-heating effect (SHE). We also provide a statistical sampling of 22FDX® MOSFETs at 4.2K using an on-chip matrix and show the first coupled double quantum dot (DQD) generated in a qubit fabricated solely on commercial FDSOI.

A. *Cryo-CMOS metrics*

Fig.2 shows the transconductance (g_m), output conductance (g_D) and intrinsic voltage gain ($A_V = g_m/g_D$) at $V_{GT} = V_{GS} - V_{TH} = 200mV$ for devices with different dimensions (channel length, L and width, W) operating at 300K (RT, red) and at 4.2K (LT, blue). As g_m is primarily determined by the effective mobility (μ_{eff}) [8], an increase of 3-5x is measured from RT and LT for the long L devices, depending on W. On the other hand, the behavior of g_D is dictated by a combination of μ_{eff} and channel length modulation. Since both g_m and g_D are proportional to μ_{eff}, the mobility effect is not reflected in A_V. The reduction of short channel effects (SCE) for longer L improves g_D, and thus A_V, with increasing L at both 300K and 4.2K. The small differences we observe in A_V with T could be explained by SHE, as will be discussed later. For L = 150nm, we measure a voltage gain of around 39dB at both LT and RT, which is on par with reported values for FDSOI [9].

Back-gate voltage (V_{BG}) in FDSOI technology allows for dynamic control of V_{TH}, enhancing performance and reducing power consumption [2, 10]. Forward back-biasing (FBB) is an important ally for cryo-CMOS circuits and can be used to decrease V_{TH} at 4.2K back to its RT value. For 22FDX® EOT-2, a FBB = 0.9V at 4.2K was needed to recover the RT V_{TH}. Fig.3 shows the $g_m(V_{GS})$ of a long L device at RT and LT which displays a parasitic hump with FBB and is indicative of ISS [11]. Consequently, for V_{GS} values around the transition from one- to two-subband conduction, (around the hump), g_m can be lower than at $V_{BG} = 0V$. Short-channel devices in comparison typically do not display ISS due to other dominant scattering mechanisms (neutral scattering induced by the source and drain, and ballistic transport) [11]. Therefore, there is a balance to be struck when choosing the dimensions and bias conditions of cryo-CMOS transistors: longer devices present lower SCE and higher A_V but are more likely to suffer from ISS.

Another important aspect to consider in cryo-CMOS design is self-heating. Shorter L devices deliver more current and therefore can suffer from stronger SHEs, which can be even more significant at LT. Fig.3 shows the $I_{DS}(V_{DS})$ at 4.2K for L = 100nm and strong V_{GT}. The negative slope in saturation regime observed in Fig.3 is one of the signatures for SHE that must be considered while designing cryo-circuits: at reduced L, both SCE and SHE degrade g_D and therefore A_V at 4.2K.

Figs.4 and 5 show the temperature increase (ΔT) due to power dissipation in FDSOI CMOS transistors. Fig.4 focuses on low input power at 4.2K and shows that $\Delta T \approx 20K$ for 100µW. Fig.5 focuses on a wider input power range and T-dependence, showing that ΔT significantly increases at LT (w.r.t. RT). This increase is due to the reduction of the Si and SiO_2 thermal conductivities, which hinder heat dissipation within the device. Notably, this behavior occurs irrespective of applied V_{BG}, and so FBB can be used to reduce power consumption, as in [10]. While the data here only shows the direct effects on the performance of cryo-CMOS analog blocks, in a QSoC, it may also severely degrade the functionality of spin qubits.

Finally, device variability must be considered in a QSoC design

kit. To enable statistical sampling, we have designed on-chip matrices in standard 22FDX® [12]. Fig.6 shows an increase of NMOS V_{TH} variability at LT w.r.t RT (1.29 *vs.* 0.93mV·µm) and no significant change in noise ($SV_G \approx 10^{-11}V^2 \cdot \mu m^2/Hz$ @10Hz). These results are compatible to the expected values for SoA 22FDX® [3] and confirm the interest of using multiplexed circuits to acquire LT statistics. Fig.7 shows characteristic Coulomb diamonds in 2D $I_{DS}(V_{DS},V_{GS})$ maps for four small MOSFETs obtained using the same matrix. The variability in the patterns (diamonds) of these maps suggests that reproducible electrostatic quantum dots (QDs) cannot be achieved with standard MOSFETs. This is likely due to the proximity of the QDs to the source/drain regions (reservoirs), where they are exposed to dopant diffusion and a non-uniform electrostatic environment.

B. Quantum dots in a 22FDX® qubit device

To circumvent random dopant diffusion and uneven electrostatic landscapes, multi-gate devices consisting of three gates in series (G1, G2, G3) and two access gates (AGL and AGR) were fabricated on the same chip as the matrices and many of the individual MOSFETs presented in section III.A. The access gates allow the QDs to be formed far from the reservoirs and control the loading of carriers inside the array. Fig.8 shows $\sigma_{VTH} \approx 75mV$ (2.4mV·µm) for $I_{DS}(V_{GS})$ curves for 35 dies measured across a 300mm wafer at RT. The 2D map of $I_{DS}(V_{G2},V_{G3})$ in Fig.8 shows features of two QDs coupled to one another. These results present the first DQD integrated on a commercial platform with no deviation from the standard process flow (*i.e.*, no impact on the digital and analog bricks).

IV. FDSOI QUBIT DEVICES

In this section we show our electron and hole single spin qubits implemented in FDSOI with different linear architectures (face-to-face gates, FF, and series gates, SR). We also show the latest generation of our FF and SR devices, consisting of four gates with integrated J-gates for tunnel coupling control. We end with some insights provided by simulations as well as stability metrics to be considered for large-scale quantum computers.

A. Single-qubits

To achieve high-contrast, single-qubit operation, our FF and SR qubits contain both a trapping potential and an electrometer. Fig.9 shows an electron spin qubit with manipulation performed by a micromagnet in an FF device, as in [4, 13]. Using electric-dipole spin resonance (EDSR), Rabi oscillations are observed for a single electron, which is placed in a magnetic gradient and displaced using an electric field created by the confining gate. When the displacement frequency matches the Zeeman energy induced by a static magnetic field, the spin of the electron oscillates with a frequency proportional to the gradient strength. Fig. 9 also shows a coherence time of 40µs after a Hahn echo sequence (w.r.t. 500ns without echo). While the decoherence time is limited by hyperfine interaction at low frequency, a Hahn echo sequence allows the suppression of these slow fluctuations and brings the qubit into an electrical noise limited coherence regime, approaching the SoA [14].

In the same technology, Fig.10 shows a hole spin qubit implemented on an SR device with 4 gates in series. Featuring strong spin-orbit interaction, holes allow spin manipulation through a local electric field without needing additional elements (contrary to the above-mentioned micromagnet). Fast readout is obtained using spin-to-charge conversion, where the charge readout fidelity is estimated to be 99.93% for 1µs integration time. This manipulation speed is similar to SoA Si/SiGe devices [15].

B. Tunnel coupling control in double quantum dots

One challenge for two-qubit gate operations in spin qubits is the control of t_c between neighboring QDs. We show that our latest qubit devices promote the required tuning thanks to the integration of J-gates [16]. A DQD stability diagram in the few-electron regime can be found in Fig. 11, demonstrating our ability to attain the charge regime required for QC. In Fig. 12 we show our ability to isolate this DQD from reservoirs and control the charge occupation, while Fig. 13 confirms our control of t_c over orders of magnitudes in both the few- and many-electron regimes. Combined with the manipulation capabilities demonstrated in section IV.A, FDSOI qubits are well-positioned to scale up the system.

C. Numerical Simulations

3D device simulations were done using a Poisson's-Shrodinger solver relying on the Effective Mass Approximation and show good agreement with t_c experiments (Fig. 14). The deviation at low t_c is likely due to charge noise, which is not currently included in our simulation model. A major challenge for spin qubits is the variability of the QD position. In Fig. 15, we show how V_{BG} can serve as a useful control knob for t_c; notably, the efficiency of t_c control is enhanced with thicker Si channels. We then analyze the impact of V_{BG} and Si thickness on variability, showing the effect on QD position along the Si channel when there is an Si/SiO_2 interface trap density (D_{it}) of $5\times10^{10}cm^{-2}$. Fig.15 shows that V_{BG} has strong impact on QD's position variability and working at reverse back-biasing is preferable. Remarkably, variability is independent of Si thickness, implying that thick channels are best to ensure a stiff control over t_c.

D. Charge noise and reliability

BTI and LFN are two good measures of qubit device stability, which is important to enable the development of large-scale, fault-tolerant quantum systems. As a critical reliability issue in semiconductor devices, BTI-induced fluctuations do not vanish at LT, despite a reduction in thermal-activated events [17]. Fig. 16 shows that under stress, BTI can reach tens of mV after a few seconds but fully recovers. The gate voltage ranges used to operate the qubit devices are reduced under FBB, which will improve device reliability. As previously observed in literature [18], Fig.16 also shows that FBB can improve LFN by pushing the carriers to the middle of the channel (*i.e.*, further away from the Si/SiO_2 interfaces). A compromise must therefore be made between stability and variability when choosing an operating V_{BG}.

V. CONCLUSIONS

Successful co-integration and deployment of large-scale quantum processors will rely on innovations in low-power circuit design, the reduction of heat generation/propagation, and efficient cryogenic cooling. We show that physical effects such as ISS and SHE become more important at LT and must be considered while designing analog blocks. The modulation of V_{TH} promoted by FDSOI can therefore be key to power optimization.

CMOS-based qubits also offer the advantage of ambipolar qubit systems, where electron and hole spin qubits can be co-integrated for different bricks. In an ambipolar FDSOI platform, we fabricated SoA electron and hole spin qubits. This paves the way for system optimization, leveraging both the long decoherence time of electrons (ex – quantum memory) and the strong spin-orbit interaction of holes (ex – fast data processing) in a single QSoC. Our findings suggest that an FDSOI QSoC platform could play a pivotal role in overcoming the scalability hurdles faced by current QC systems.

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Franck Barzic for measurements support. Félix Beaudoin and Pericles Philippopoulos from Nanoacademic for QTCAD® simulation collaboration and support. This work was partly supported by the French National Research Agency under the program "France 2030" (PEPR PRESQUILE - ANR-22-PETQ-0002), and the European Research Council (ERC) Synergy QuCube project (grant. n. 810504).

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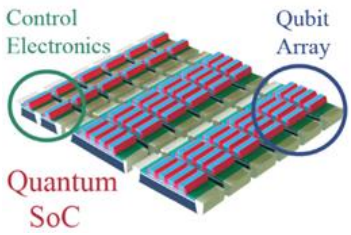

Fig. 1. Schematic of control electronics and quantum bits using FDSOI technology. The proposed architecture for the qubits consists of linear arrays with 4 gates in series, our standard cell for future two-qubit gates.

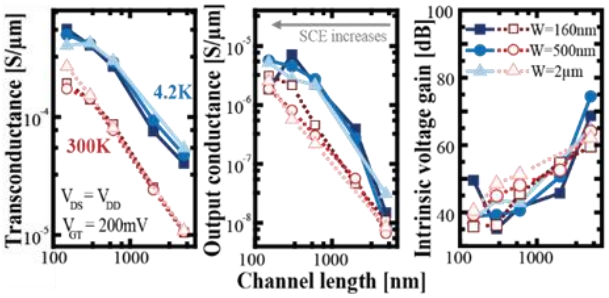

Fig. 2. Analog parameters transconductance (g_m/W), output conductance (g_D/W) and intrinsic voltage gain (A_V) varying the channel length and channel width, at 300K and 4.2K, V_{BG} = 0V.

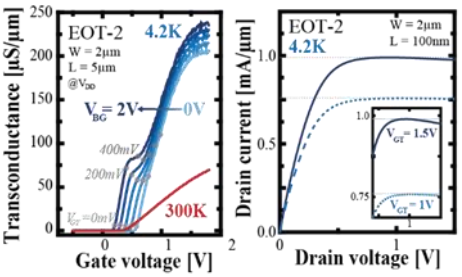

Fig. 3. (left) g_m/W vs. V_{GS}, varying V_{BG} for long channel length at 4.2K. **(right)** I_{DS}/W vs. V_{DS} varying the gate voltage overdrive (V_{GT}), for short channel length at 4.2K

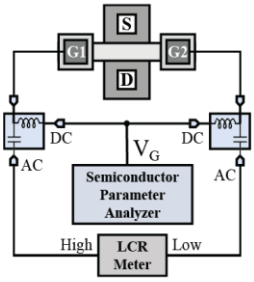

Fig. 4. (left) Schematics of the gate thermometry test structure and measurement setup. **(right)** ΔT vs. input power for n- and pMOS at ambient temperature of 4.2K.

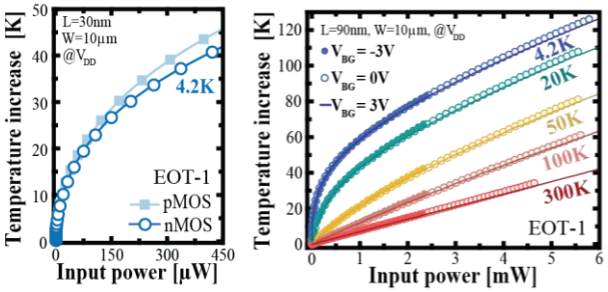

Fig. 5. ΔT vs. input power varying ambient temperature and V_{BG} for nMOS operating in saturation.

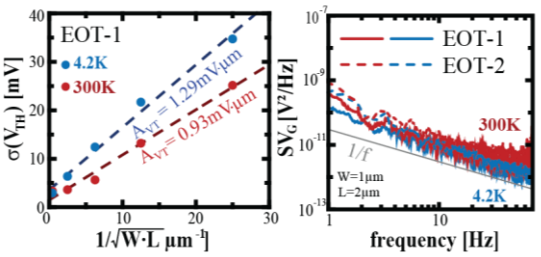

Fig. 6. (left) Pelgrom plot (28 devices per dimension) and **(right)** LFN obtained using an on-chip addressing matrix at 300K and 4.2K.

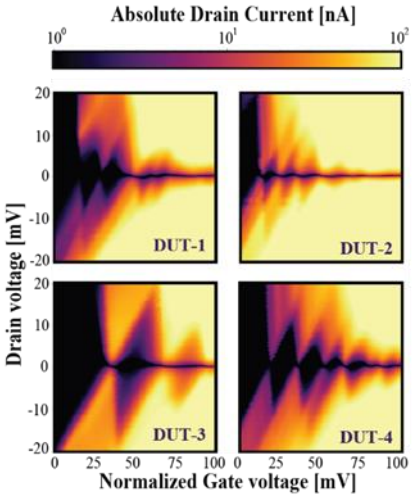

Fig. 7. Example of statistics for Coulomb diamonds measured using addressing matrix. DUTs consist of commercial 22FDX® MOSFETs with W = 80nm and L = 22nm.

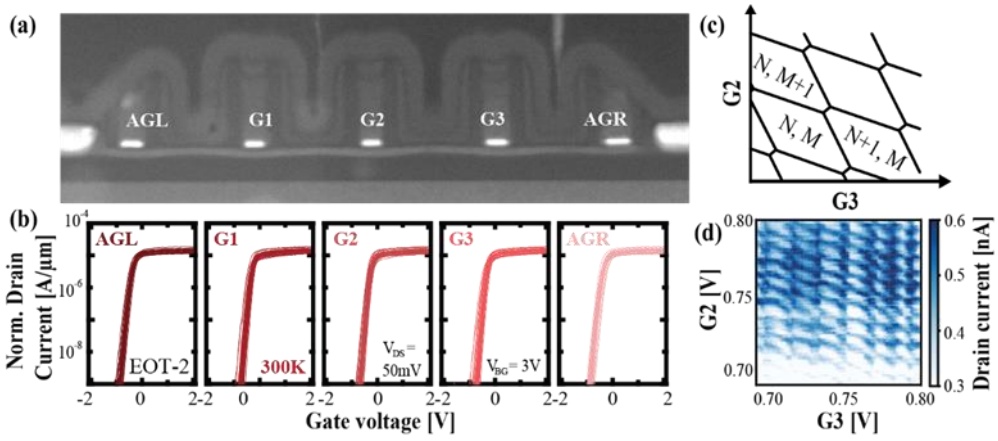

Fig. 8. (a) TEM cross-section of a qubit device in 22FDX® with 3 gates (G1-G3) and 2 access gates (AGR, AGL). **(b)** Room temperature I_{DS}/W vs. V_{GS} statistical sampling on 35 dies, collected at center, middle and edge of wafer. **(c)** Theoretical stability diagram for two capacitively and tunnel coupled quantum dots. **(d)** Measured stability diagram showing two coupled quantum dots in a 22FDX® *n*-type qubit.

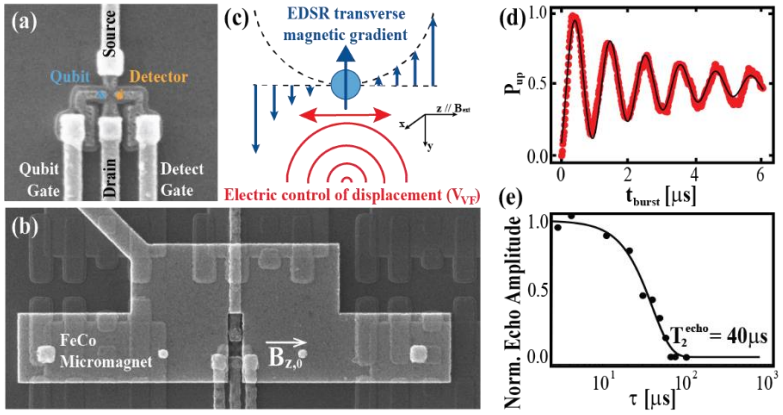

Fig. 9. Electron spin qubit. **(a)** and **(b)** SEM image of the FF device with post processes including contacts and micromagnet. **(c)** Principle of EDSR. **(d)** Rabi oscillations of a single electron using EDSR, at 1MHz in a gradient of 0.1mT/nm and voltage excitation of 1mV on the confining gate. **(e)** Result of a Hahn echo sequence showing the evolution of the coherence vs. the total free evolution time.

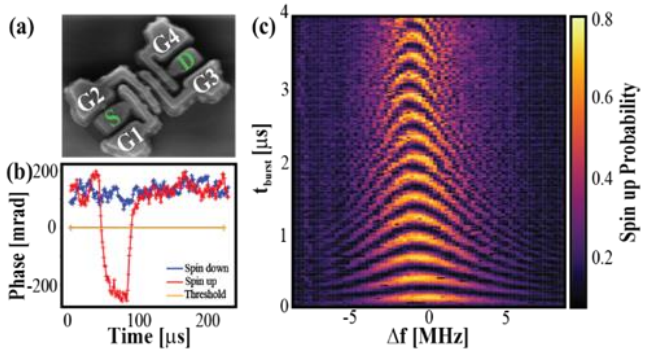

Fig. 10. Hole spin qubit. **(a)** SEM image of SR device. **(b)** Time traces measured through an Elzerman-type readout. Some traces present a jump in the phase signal, inferring that a tunnel event occurred, hence a spin up is measured. In these devices, we achieved charge readout fidelity as high as 99.93% at 1μs integration time. **(c)** Spin up probability measured by energy-selective readout, as a function of burst time and frequency detuning, with respect to 17 GHz.

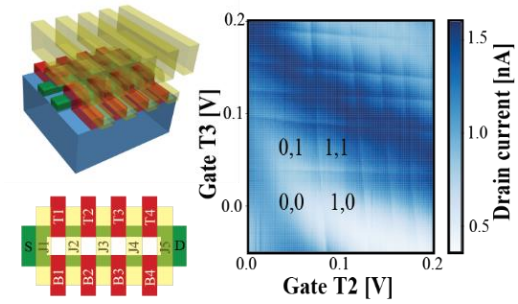

Fig. 11. (left) Schematics of 4 gates in FF configuration with split channels and J-gate integration. **(right)** Charge detection of DQD in the few-electron regime. The charge detector is a single-electron transistor (SET) located at the bottom wire. The DQD is located underneath gates T2 and T3, at the top wire. Although the DQD is isolated from the SET, it is still tunnel coupled to both reservoirs via gates T1 and T4, both open at 2V. The numbers inside the 2D map indicate the charge occupation of the two dots (i.e. 1,1 refers to one electron in each QD).

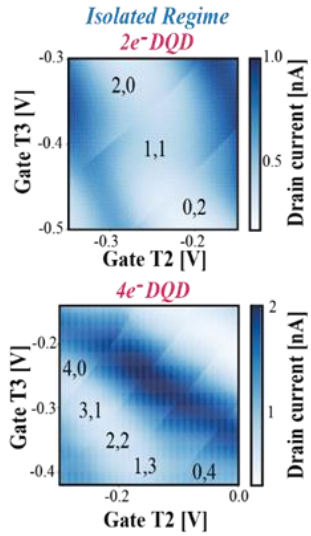

Fig. 12. Isolated regime of 2 and 4 electrons in a DQD. The diagonal lines delimit the charge states of the QDs. These charge configurations can be used for 2-qubit gates.

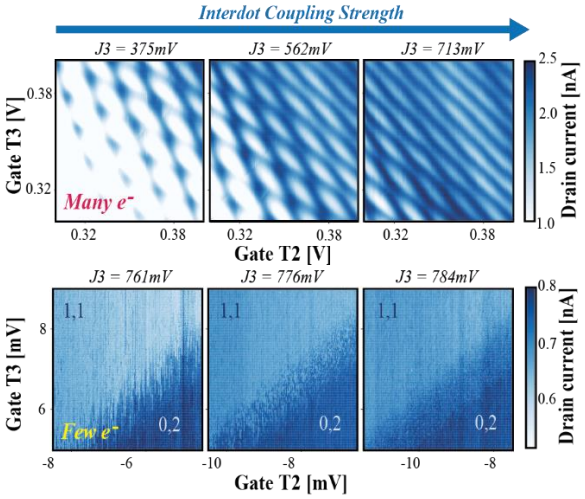

Fig. 13. Qualitative tunnel coupling control in the many **(top)** and in the few **(bottom)** electron regime using the barrier gate between the DQD J3. In the few-electron regime, t_c modulation is observed through the change in frequency for the stochastic events in the transition between (1,1) and (0,2), which indicates that one electron is tunneling from QD1 to QD2.

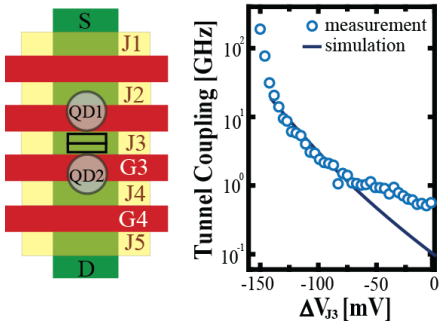

Fig. 14. Hole SR devices. Evolution of the interdot tunnel coupling of an isolated DQD with respect to the associated J-gate. The interdot transition is measured with gate reflectometry and fitted to extract the tunnel coupling. Simulation shows good agreement with measurements on a decade tuning range.

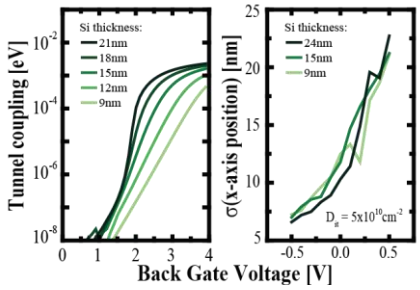

Fig. 15. Simulation data for tunnel coupling and variability of QD position along the channel length vs. back-gate voltage. D_{it} = 5×10^{10}cm^{-2} at both front and back Si/SiO$_2$ interfaces.

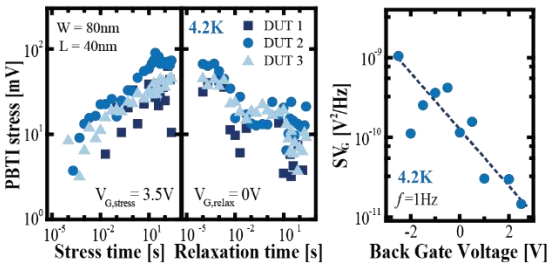

Fig. 16. PBTI **(left)** and LFN **(right)** measured at 4.2K. Both parameters are used to evaluate the devices stability and demand specific optimization w.r.t. to CMOS to allow for high fidelity qubit operations. A dotted line in **(right)** to guide the eye. Noise was measured at the edge of a Coulomb peak.